THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 50, No. 4, April, 1971
*Printed in U.S.A.*

## Statistical Circuit Design:

# A Monte Carlo Tolerance Analysis of the Integrated, Single-Substrate, RC, *Touch-Tone*® Oscillator

By P. BALABAN, B. J. KARAFIN and MRS. D. B. SNYDER

(Manuscript received November 30, 1970)

*Monte Carlo tolerance analysis has proven to be an effective tool in evaluating the sensitivity of a circuit design to manufacturing tolerances and environmental changes. Such an analysis involves repetitively "constructing" samples of the design in the computer, randomly selecting parameters that obey the manufacturing statistics; "tuning" the samples; and analyzing their operation under "field conditions." At the conclusion of this process one is able to form empirical distributions of circuit performance, to predict yield, evaluate tuning procedures, etc.*

*This paper describes a Monte Carlo study of two proposed designs for an integrated, single-substrate, RC,* Touch-Tone® *oscillator. Difficulties arise in perfoming this study because (i) the statistics of integrated circuit components are closely correlated, and (ii) the inherent nonlinearity of oscillators coupled with tight circuit performance specifications require tailored analysis techniques.*

*The study shows one of the two designs to be superior. A lower bound of 55 percent yield is predicted for this design, and a simple test for eliminating oscillators that fail to meet requirements is presented. Low transistor current gain is shown to be a dominant cause of failure. Lastly, asymmetry in the effects of impairments on circuit performance suggest a modification in adjustment strategy.*

### I. INTRODUCTION

The effective design of a circuit that will be mass-produced and subjected to a wide range of environmental conditions must go beyond the specification of a nominal circuit. It must include consideration of performance deviations due to parameter variations stemming

from manufacturing tolerances and environmental changes. Bounding these performance deviations is often the most difficult part of the design process.[1]

Monte Carlo tolerance analysis has proven to be a useful tool in dealing with these broader design questions. The approach, which is depicted in Fig. 1, simulates on a computer the process of picking a random sample of manufactured circuits, following these circuits through factory adjustment, monitoring their operation under field conditions, and compiling statistics on circuit performance.[2,3] Note that the Monte Carlo approach obviates the need for linearizing assumptions that characterize many other techniques for viewing product performance (worst-case, first-order sensitivities, etc.). It should be remembered that the response of even a linear circuit is a nonlinear function of its parameters.[2]

This paper contains the results of a computer tolerance analysis of two integrated, single-substrate, *Touch-Tone* oscillators. Section II describes the two designs and lists the performance specifications that must be met. The study produces distributions of oscillator frequency, amplitude and other measures for the various modes of circuit operation at several values of temperature. When these distributions are considered in the light of allowable degradations, several questions can be answered:

(*i*) Yield can be predicted. By yield we mean the ratio of circuits that will meet all field requirements to the total number produced without catastrophic failure. Computer simulation cannot include, for example, those cases where chips are damaged in handling or where silicon imperfections result in circuits being discarded.

(*ii*) Factory tests can be devised to insure that factory yield matches true yield. In other words, tests are devised such that the factory neither ships circuits that will fail in the field, nor discards those that would be acceptable. In the case where extremes of tem-

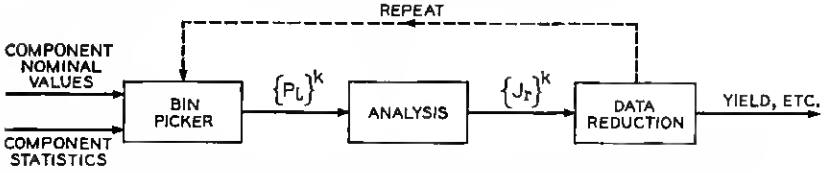


Fig. 1—Monte Carlo tolerance analysis. $\{P_i\}^k$, set of parameters for $k$th sample circuit; $\{J_r\}^k$, set of performance indices for $k$th sample circuit.

perature are encountered in the field, an effective but expensive factory test facility would involve a temperature chamber. The results of the study presented below indicate that a test on a secondary criterion (dc feedback current) at room temperature is an acceptable test of circuit performance over the full temperature range.

(*iii*) The parameter deviations that cause circuit failure can be identified. This information indicates where efforts to improve fabrication techniques should be concentrated.

Integrated circuits in general accentuate the need for automated tolerance analysis. The long turnaround time for masks and models and the expense associated with design changes make the ability to study such changes on the computer attractive, especially when one is interested in the implications of a change on manufacturing yield and field performance. In the particular case of a *Touch-Tone* oscillator whose production rate might exceed a million per year, accurate prediction of yield is vital in determining the economic feasibility of a design.

Unfortunately, while integrated technology increases the need for automated tolerance analysis, it also makes that analysis more difficult to perform. At each iteration of the Monte Carlo loop shown in Fig. 1, the block labeled "Bin Picker" must produce a set of parameters from which one sample circuit can be "built." Implementation of the "Bin Picker" is straightforward for discrete circuits. In that case, parameters are independent and the box is implemented by using random number generators to select element values from their individual distributions. By contrast, the parameters of a silicon integrated circuit are *not* independent. In fact, every element on the chip is correlated with at least every other element of the same kind, e.g., the $\beta$s of all transistors on the same chip are correlated with one another. It is a familiar fact that while a given resistor on a chip may vary by $\pm 15$ percent from nominal, the ratio of any two resistors will vary by only $\pm 5$ percent from nominal. It would not do, therefore, for the Bin Picker to select silicon resistors from distributions with limits of $\pm 15$ percent. The Bin Picker must be concerned with both global statistics (the distribution of parameter values across the population of manufactured circuits) and chip statistics (the relationship of parameter values on any given chip).

A comprehensive treatment of the statistical characterization of integrated circuits appears in Ref. 4; comments particular to the *Touch-Tone* oscillator are contained in Section III below.

While the fact that the *Touch-Tone* oscillator is an integrated circuit complicates the Bin Picker, its nonlinear character presents difficulties in the implementation of the Analysis box of Fig. 1.* The analysis of linear circuits is accomplished by algebraic manipulations, a task at which the digital computer is fast.[2] Nonlinear circuits, on the other hand, require the integration of the differential equations describing the circuit. Unfortunately, the digital computer is slow at this task.[3] The problem is complicated further by tbe fact that the system of differential equations describing the *Touch-Tone* oscillator is stiff, i.e., has eigenvalues differing by several orders of magnitude. This is not surprising since we have a kHz oscillator built with MHz transistors. Although efficient algorithms have recently been developed to handle stiff systems of differential equations,[5] analysis of a single oscillator at a single temperature that provides sufficient accuracy to determine whether or not the rather stringent design requirements (e.g., ±0.1 percent frequency deviation due to amplifier variations) are met requires in excess of *ten hours* of computer time on a CDC 3300. Since several hundred oscillators will have to be analyzed at a number of temperatures, such an analysis time for a single oscillator is unacceptable. Special analysis techniques, therefore, had to be developed for the *Touch-Tone* oscillator study. These techniques, which are described in Section IV, reduce the analysis time for a single oscillator to about 3 minutes.

The results of the tolerance study are presented in Section V. Histograms of oscillator frequency and amplitude are presented at −40°C and +60°C, the temperature extremes expected in the field. Further, the change in amplitude with frequency selection is discussed. The oscillator is designed to generate four tones, corresponding to different user selection of dial digits. The change in amplitude with "button-seleetion" is significantly different from what one might expect by looking at the oscillator as a quasi-linear system. Finally, the implications of using a dc feedback current measurement at room temperature as an oscillator acceptance test is discussed.

It should be kept in mind that while this paper is concerned primarily with the computer study of the single-substrate, *Touch-Tone* dial, that study has been carried on in parallel with laboratory testing of breadboards and models. The extent to which these two approaches—laboratory and computer—have complemented one another cannot

* Oscillators are inherently nonlinear; some phenomenon must be present to limit the amplitude of oscillation.

be overemphasized. In many instances the direction of the computer study was influenced by effects observed in the laboratory, and vice versa. Further, the assumptions and many of the qualitative results detailed below have been corroborated experimentally.

## II. THE OSCILLATORS AND THEIR REQUIREMENTS

The dial incorporated in the Bell System *Touch-Tone* telephone contains two multifrequency audio oscillators to perform the dialing function. These oscillators and the associated switching are used to generate appropriate frequencies (a unique pair for each button on the dial) for dial switching information.

In this paper we study two RC, single-substrate, integrated oscillators that have been proposed as replacements for oscillators currently in use.

Each RC oscillator contains a nonlinear active device, a Twin-T feedback network and a buffer stage for connection to the telephone line (Fig. 2). The Twin-T portion of the oscillator is a tantalum, thin-film circuit whose schematic and voltage transfer ratio are shown in Figs. 3a and b, respectively. The notch depth of the voltage transfer characteristic is adjusted to −37 dB. The oscillator is designed to produce tones of four separate frequencies. The switches, S1 to S4, in Fig. 3a are used to select the different frequencies by changing the value of $R_2$. The Twin-T is so designed that the changes in $R_2$ have only a small effect on notch depth.

The nonlinear active device is an integrated silicon dc-coupled amplifier with a built-in limiter. Figure 4 shows the voltage transfer characteristic of such an amplifier. To sustain an oscillation, the

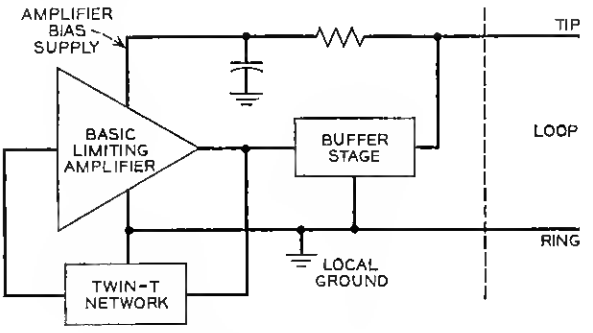


Fig. 2—Basic oscillator configuration.

slope of the amplifier transfer characteristic (gain) in the vicinity of the steady-state operating point must exceed 37 dB—the loss of the Twin-T network. The limiting voltage ($E_{LIM}$) of the amplifier must be controlled so that oscillator amplitude can be controlled. $E_{LIM}$ is controlled by a tantalum resistor on the same substrate as the Twin-T network that is anodized during oscillator adjustment.

After an amplifier chip is bonded to the thin-film circuit, each component of $R_2$ in the Twin-T circuit is adjusted at room temperature so that each of the four tones is within $\pm 0.2$ percent of its nominal frequency. Once the frequencies have been adjusted, deviations in each of the four frequencies from their tuned values due to amplifier changes over a temperature range of $-40°C$ to $+60°C$ must be within $\pm 0.1$ percent.

Amplitude of oscillation at one of the four tones is also adjusted at room temperature to within $\pm 0.5$ dB of its nominal value. The deviation in the amplitude of the adjusted tone must be less than $\pm 1.0$ dB due to temperature-induced changes in the amplifier. Further, the range of amplitudes of the four tones must be within $\pm 1.0$ dB at any temperature. One way of viewing these requirements is to say that oscillator amplitude must be within $\pm 2.5$ dB from nominal over the full temperature and tone frequency ranges.

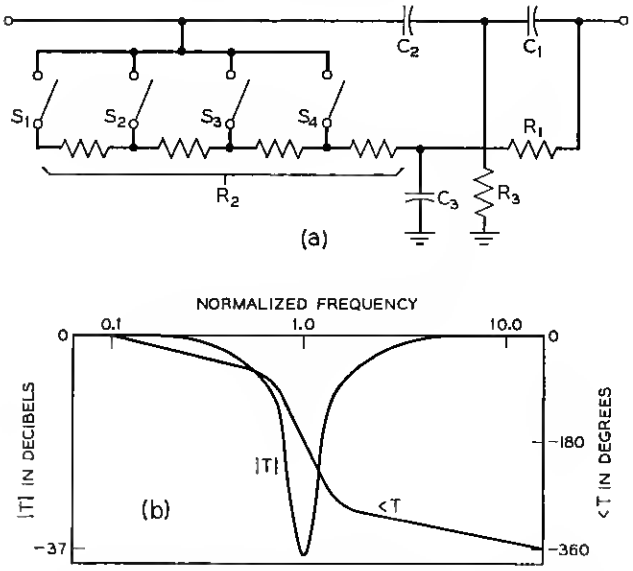


Fig. 3—(a) Twin-T schematic, (b) Twin-T no-load transfer ratio.

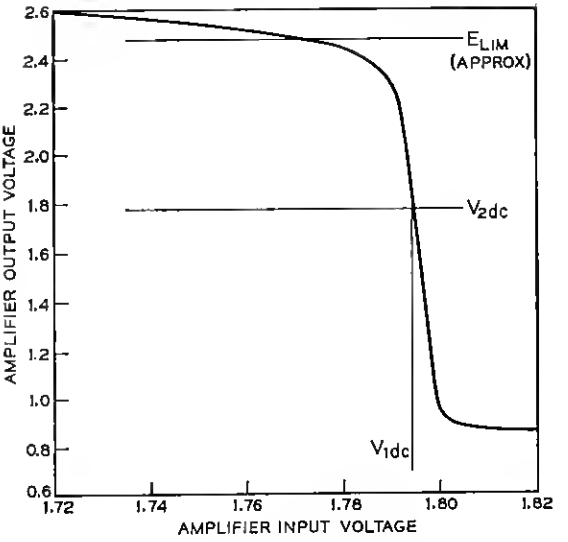


Fig. 4—Typical amplifier static transfer curve.

Requirements are quoted in terms of temperature effects on the amplifiers since the two designs under study differ only in the amplifiers used. It is possible, therefore, using the computer, to hold the Twin-T at nominal temperature while subjecting the amplifier to the full temperature range and thus separate out deviations due to amplifier sensitivity.

To achieve the required amplitude and frequency stability (as well as low distortion), the amplifier should exhibit: (*i*) high ac input impedance, (*ii*) low ac output impedance, (*iii*) small dc input current, and (*iv*) constant gain in the linear region.

Schematics of the two amplifiers (henceforth called A and B) are shown in Figs. 5 and 6. Both amplifiers achieve limiting via nonlinear feedback: In Amplifier A, transistor $Q_3$ is cut off until the output voltage divided by the $R_1R_2$ voltage divider is sufficient to turn it on. In other words, $Q_3$ is cut off in the high gain region, but provides limiting when it goes active. $R_2$ is a tantalum resistor that can be adjusted to control the limiting point and hence the oscillator amplitude. In Amplifier B, transistor $Q_6$ is cut off in the high gain region and is turned on when the output voltage divided by the $R_8R_{91}R_{92}$ voltage divider is high. $R_{92}$ is tantalum and is used to adjust oscillator amplitude. The basic differences in the amplifiers are that B has substan-

tially higher input and lower output impedances than A. Furthermore, while the input impedance of A degenerates in the limiting region, the input impedance of B is held at a high level by the feedback provided by $R_5$. The input impedance of B drops off only when $Q_4$ goes into cutoff, a condition that is avoided by keeping the oscillator gain margin relatively low.

It should be clear that the above discussion is qualitative. For example, it is difficult to make precise statements about the effects of low input impedance of Amplifier A in the limiting mode. Furthermore, both amplifiers are satisfactory when built with nominal device parameters. It is left to the computer tolerance analysis to supply data with which to compare the two designs when subjected to manufacturing tolerances and temperature extremes.

## III. THE VARIATION OF PARAMETERS

In the simulation each iteration of the Monte Carlo loop shown in Fig. 1 represents the "building" of one sample oscillator. The circuit's nominal parameters at 20°C are altered by techniques described in Ref. 4 using appropriately shaped random number generators and the device fabrication statistics. The circuit "built" with these altered parameters is then put through a simulation of the adjustment procedure to arrive at values for the adjustable elements. At this point

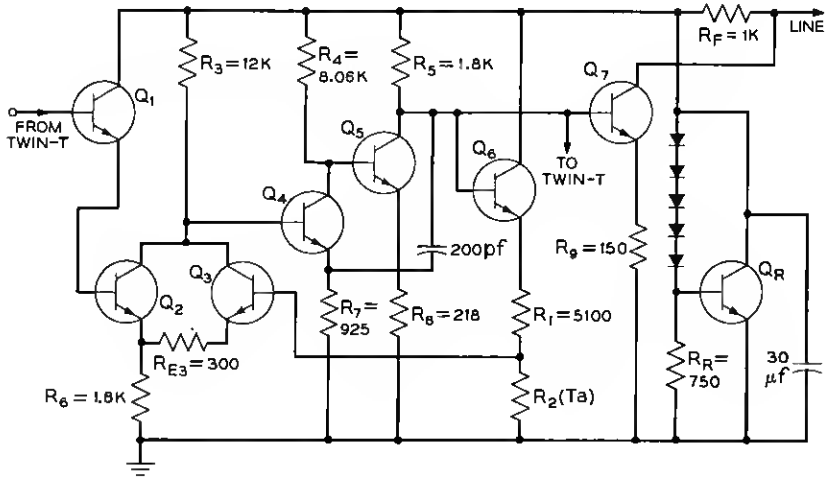


Fig. 5—Amplifier A schematic.

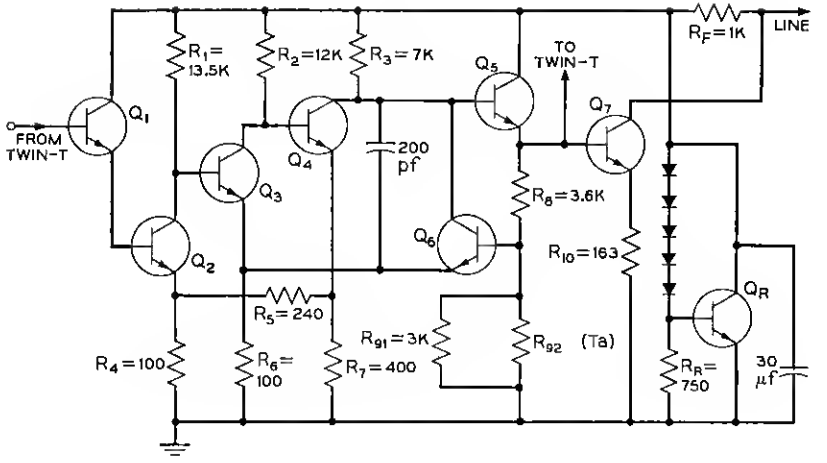


Fig. 6—Amplifier B schematic.

we have a realistic sample circuit that is ready for "installation in the field." Its operation at 20°C is analyzed; frequency, amplitude, loop current, etc., are noted. The parameters are then again altered in accordance with their temperature behavior to simulate circuit operation at other temperatures of interest. Further, at each temperature, the variable arm resistor of the Twin-T is stepped through four values to allow simulation of the production of the oscillator's four tones.

In the *Touch-Tone* oscillator study, the parameters of the tantalum Twin-T network are held fixed at their nominal values at 20°C, while the parameters of the amplifier are chosen in accordance with expected statistical manufacturing variations and subjected to temperatures of −40°C, +20°C and +60°C. (The change in performance of a given realization of either of the oscillators is expected to be monotonic with temperature. Therefore, the oscillators are tested at nominal and at the extremes of the temperature range of interest.) This line of attack is taken so that oscillator degradations due to the amplifier imperfections can be isolated; performance and influence of the Twin-T components are relatively well understood. With the exception, then, of the tantalum adjustment resistor, the parameters that the Bin Picker is concerned with are those of the silicon, integrated amplifier.

Further, the silicon amplifiers are treated as infinite-bandwidth devices. The amplifier capacitors, both inside and outside the transistors, are ignored. Hence, the amplifiers are modeled as networks of

resistors and Ebers-Moll dc transistors.[4] The parameters that are subjected to Monte Carlo perturbations and vary with temperature are: (*i*) transistor forward current gain, $\beta_N$; (*ii*) silicon resistors, $R_S$; (*iii*) base resistors, $R_B$; and (*iv*) collector and emitter intercept currents, $I_{CS}$ and $I_{ES}$. In normal operation of either amplifier, no transistor is in saturation. Therefore, it is assumed that effects of variation in the reverse current gain, $\beta_I$, are negligible, and so $\beta_I$ is held constant for all transistors, $\beta_I = 1$.

It is clear that the results of the Monte Carlo study are only as accurate as the characterization of the manufacturing and temperature variations of the above parameters. Unfortunately, statistical data for silicon, integrated circuits is very sketchy. The data used for this study is a combination of (*i*) data on "similar" transistors, (*ii*) measurements of a limited number of *Touch-Tone* devices, and (*iii*) some educated guessing by the device designers and modelers. Because of the uncertainty in the data, no attempt has been made at rigorous statistical characterization of the silicon process. Instead, coefficients were estimated for the assumed mathematical model such that the silicon parameters, spreads, and correlations produced by the Bin Picker "match" what measurement data exist and are consistent with what is expected by the device designers.

The precise distributions, correlations, temperature coefficients, etc., that were used in this present study may be found in the more thorough discussion presented in Ref. 4.

## IV. ANALYSIS

Both amplifiers under study are very broadband. Since the intended frequencies of the oscillators are below 2 kHz, the amplifiers are assumed to be of infinite bandwidth. The amplifiers are thus treated as nonlinear, memoryless, two ports; all capacitances, both those intrinsic to the transistors and those added to suppress high-frequency oscillations, are ignored. The amplifiers are then analyzed as networks of resistors and Ebers-Moll dc transistors.

The nonlinear two-port, Fig. 7, can be characterized by:

$$\begin{aligned} v_2 &= f_1(v_1, i_2), \\ i_1 &= f_2(v_1, i_2). \end{aligned} \tag{1}$$

Since the output current of both amplifiers is small, we can use a Taylor series expansion of (1) around $i_2 = 0$. Keeping the first two terms of the expansion of the first equation, we have


Fig. 7—Nonlinear two-port.

$$v_2 \approx f_1(v_1 , 0) + \left.\frac{\partial f_1}{\partial i_2}\right|_{i_2=0} i_2 . \tag{2}$$

The first term is the open circuit voltage gain of the amplifier, while the second term coefficient is the incremental output impedance.

The second equation of (1) is handled even more simply, since

$$\left.\frac{\partial i_1}{\partial i_2}\right|_{i_2=0}$$

the incremental reverse current gain, is near zero for most multistage amplifiers. Hence,

$$i_1 \approx f_2(v_1, 0).$$

To characterize the amplifiers it is, therefore, only necessary to compute three nonlinear functions:

$$v_{20} \equiv f_1(v_1 , 0) \quad \text{(the no-load gain function)} , \tag{3a}$$

$$i_1 = f_2(v_1 , 0), \tag{3b}$$

$$Z_0 \equiv \frac{\partial f_1(v_1 , 0)}{\partial i_2} \equiv f_3(v_1 , 0), \tag{3c}$$

each of the independent variable, $v_1$ .

Having computed these functions for each amplifier produced by the Bin Picker at each temperature, the analysis of the oscillator is carried out in a manner illustrated by Fig. 8. In words, the nonlinear

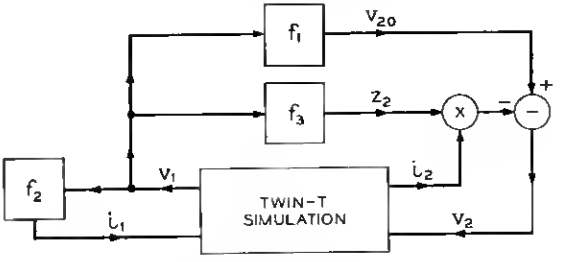


Fig. 8—Oscillator simulation.

functions describing the amplifier are used to supply the necessary port termination to the differential equations of the Twin-T. This set of differential equations, made nonlinear and implicit by the addition of the amplifier functions, are then solved using an implicit, numerical integration scheme to produce $v_2(t)$, the oscillation output, as a function of time from which oscillator frequency and amplitude can be measured.

To compute the three functions ($v_{20}$, $i_1$, $Z_0$), we proceed as follows: Fig. 9 is a block schematic of the oscillator and its environment. A fixed length is assumed for the loop (6 kft). The bypass capacitor, $C_1$, is assumed to be an ac short circuit, and hence $V_0$ is taken as a constant dc potential.* The first step is a computation of $V_0$ for each amplifier produced by the Bin Picker at each temperature. Since distortion is very low in the amplifier, the assumption is made that the dc current supplied to the amplifier in steady state is equivalent to the dc currrent supplied when the Twin-T is replaced by its series resistance.

The mesh equations of one amplifier with the dc resistance of the Twin-T in the feedback loop are written. $V_0$ is assumed an external source. The buffer transistor is added by assuming it always operates in the active region so that the collector current, $I_C$, is determined by the base-emitter junction operation. The linear equations of this set are solved leaving a set of nonlinear algebraic equations, one equation for each nonlinear junction. We will call this set of equations the basic set for the amplifier. To account for the remainder of the configuration of Fig. 9, we augment the basic set with equations that describe the regulator, the equalizer, and an equation that accounts for the second amplifier. This last equation is:

$$V_0 = E_B - (2I_S + I_R)(R_F + R_L) - (2I_C + I_H)R_L.$$

This augmented set of nonlinear algebraic equations is then solved by a norm-reducing, Newton–Raphson technique. The results of this analysis are: $V_0$ ; $V_{1\mathrm{dc}}$, the voltage at the input of the amplifier; $V_{2\mathrm{dc}}$, the output voltage of the amplifier or the input voltage to the buffer stage; and a quantity that turns out to be of special importance in analyzing the results, $I_{\mathrm{dc}}$, the current through the dc resistance of the Twin-T, i.e., the current into the input of the amplifier when the Twin-T is replaced by its dc resistance. Since output distortion of the oscillator is expected to be low, $V_{2\mathrm{dc}}$ is the "center line," or average

* Consideration of the effects of variable loop length would require inclusion of the capacitor, $C_1$, in the simulation model.

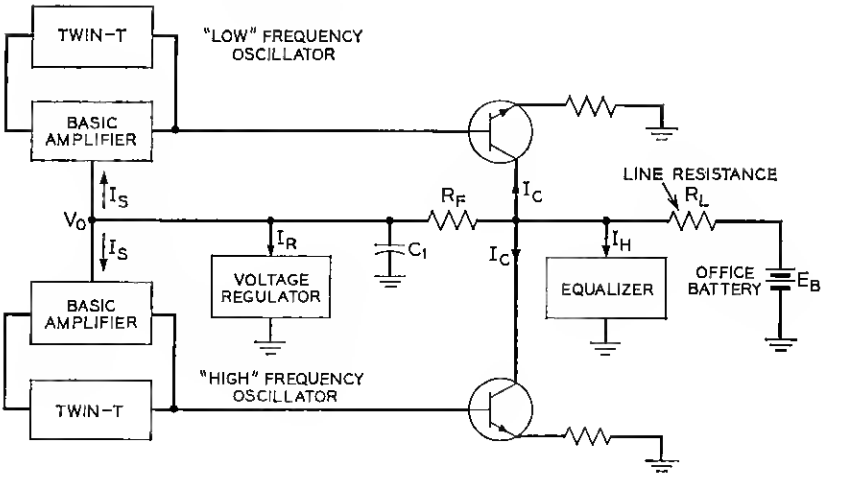


Fig. 9—Block-schematic of oscillator and related circuitry.

voltage of the oscillator output. Hence, crossings of $V_{2dc}$ are used to measure frequency during the dynamic simulation. Further, we know that in calculating three functions (3a–c), we can restrict the range of $v_1$ to include and be slightly larger than the high gain region shown in Fig. 4. The value, $V_{1dc}$ , gives us a point in the high gain region, fixing the position of that region in the range of $v_1$ . It should be noted that the high gain region shifts considerably over $v_1$ from amplifier to amplifier and from temperature to temperature. It is therefore important to fix the position of the region to minimize the necessary computation in building (3a–c).

Once $V_0$ , $V_{1dc}$ and $V_{2dc}$ are computed, we return to the basic set of equations. The dc resistance of the Twin-T is removed and a voltage source, $V_1$ , is connected between the input to the amplifier and ground. $V_1$ is then stepped in 1.5 mV increments and around $V_{1dc}$ to cover a range of 150 mV, and $v_{20}$ and $i_1$ are calculated. The process is repeated with the addition of a small current source at the output of the amplifier to compute $Z_0$ .

Once the functions (3a–c) are computed, we could proceed to the dynamic simulation of the oscillator as shown in Fig. 8, if it were not for the frequency and amplitude adjustments that must be made. These adjustments are accomplished in the following manner: Considering frequency tuning first, we realize that tuning is necessary because of manufacturing tolerances on the components of both the

tantalum and silicon circuits. Since our simulation has exact values for tantalum components, one cause of frequency deviation is removed. Further, because frequency deviations are expected to be small, we make the assumption that frequency deviations due to temperature in a given oscillator are independent of frequency tuning. In other words, for a given oscillator the frequency difference measured between +20°C (the tuning temperature) and any other temperature is independent of the actual frequency at +20°C, at least for the expected deviation between tuned and untuned +20°C frequencies. We further assume that frequency tuning has a negligible effect on oscillator amplitude. With these assumptions we eliminate the need for frequency tuning and proceed as follows. Each oscillator is simulated at +20°C. The frequency is measured; call it $f_{20}$. The difference

$$\Delta f = f_0 - f_{20}$$

is calculated, where $f_0$ is the nominal frequency. The oscillator is then simulated at other temperatures and the frequency measured to be $f_T'$. The frequency predicted for the oscillator at temperature $T$ (again accounting only for effects in the amplifier) is then

$$f_T = f_T' - \Delta f.$$

Amplitude adjustment cannot be handled so simply. In our simulation, the tantalum tuning resistor in the amplifier is actually adjusted at +20°C and at one *Touch-Tone* frequency to produce an amplitude within the tuning specs, ±0.5 dB. This is accomplished by repetitively simulating, measuring, adjusting, simulating, etc. By using a sub-loop adjustment while (3a–c) are being calculated so that $E_{\text{LIM}} - V_{2\text{dc}}$ (see Fig. 4) is the desired peak amplitude, accurate adjustment can usually be made with one iteration of the full simulation. It should be remarked that if the amplifier and Twin-T were perfectly buffered from one another, $E_{\text{LIM}} - V_{2\text{dc}}$ would be an accurate prediction of amplitude. Hence, those amplifiers for which the prediction is poor and which require more than one or two iterations of the full simulation loop are precisely those amplifiers with poor performance.

Upon completion of amplitude adjustment, the resulting amplifier functions are used in the simulation shown in Fig. 8. This dynamic simulation is run for 30 cycles of the oscillator fundamental to obtain accurate measures of steady-state amplitude and frequency.

The separation of the oscillator into an infinite-bandwidth, nonlinear amplifier and a linear frequency selective network reduced the computation time for a single oscillator by at least two orders of magni-

tude from the time required by the most efficient nonlinear circuit analysis programs.

## V. RESULTS

Monte Carlo studies were made on several versions of oscillator A, i.e., for several sets of suggested nominal parameter values. In every case the results were discouraging, i.e., only a small number of Monte Carlo samples passed the oscillator specification tests. On the other hand, the results of Monte Carlo studies on oscillator B are encouraging. The differences in the results of the studies of the two oscillators are so great that oscillator A has been abandoned as a contender for the next generation of RC *Touch-Tone* dials.

Figure 10 displays the histograms of oscillator A frequency at

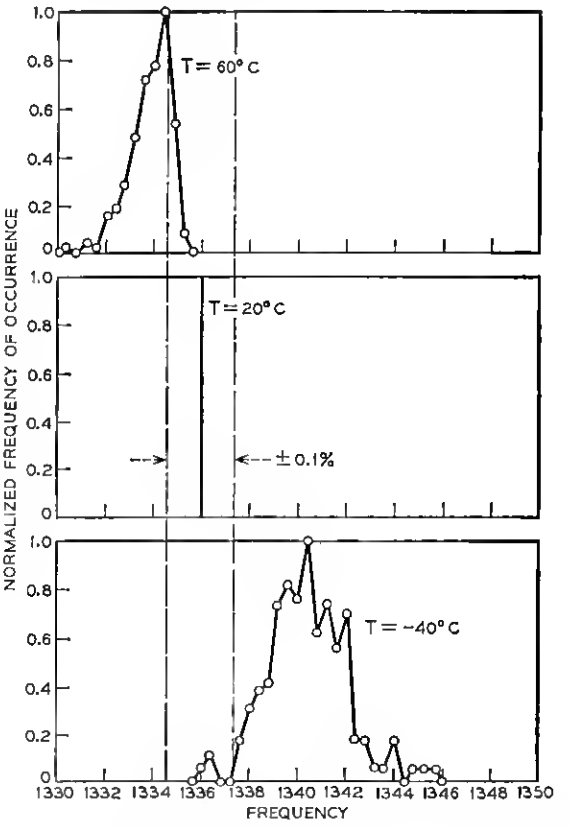


Fig. 10—Amplifier A normalized frequency histograms, $f_0 = 1336$ Hz.

60°C, 20°C, and −40°C. This histogram at +20°C is an impulse since the oscillators are tuned at this temperature. The histograms at the other two temperatures, however, show that the majority of oscillators fall outside the 0.1 percent frequency limits; only four sample oscillators, of 200 tested, were inside the frequency limits. With frequency stability this poor, further tests of the oscillator were not performed.

Poor frequency stability is explained by loading of the Twin-T by the amplifier,* loading that is largely eliminated in oscillator B. Both input and output impedances of the amplifiers under study are nonlinear, i.e., change during the oscillator cycle. Hence, no linear analysis of Twin-T loading is possible. However, by examining the extremes of these nonlinear impedances, we can make qualitative statements about frequency stability.

A typical sample of amplifier A has an input impedance that varies between 165 kΩ and 1.5 MΩ at +20°C and between 80 kΩ and 785 kΩ at −40°C. Even if these impedances were constant at their maximum values, i.e., if the input impedance of the amplifier were 1.5 MΩ at +20°C and 785 kΩ at −40°C, the change in the −180° phase point of the Twin-T is almost 0.1 percent. Changes of the −180° point at the low impedance level, i.e., between 80 and 165 kΩ, are very large. Since the −180° phase point determines the frequency of oscillation, we see that amplifier A has insufficient input impedance to provide an acceptable oscillator.

Typical samples of amplifier B, on the other hand, have input impedances varying between 900 kΩ and 19 MΩ at +20°C and between 700 kΩ and 14 MΩ at −40°C. At these impedance levels, shift in the Twin-T −180° phase point is negligible.

An additional factor is that amplifier A has output impedance as high as 1.6 kΩ while that of amplifier B is held below 250 Ω.

The preceding discussion intimates that oscillator B will be frequency stable. As we shall see below, this is correct, and although amplitude stability causes some difficulties, the Monte Carlo study predicts a lower bound of 55 percent yield for oscillator B.

### 5.1 *What is Yield?*

When dealing with integrated circuits, the word "yield" must be interpreted with caution. Tests are performed at many points in the

* This effect has been observed both with computer simulations and model tests at Bell Telephone Laboratories at Indianapolis. It has been observed further that increases in transistor $\beta_N$ increase the frequency stability of oscillator A.

multistep fabrication process with some number of circuits rejected at each test. The actual yield, i.e., the ratio of satisfactory circuits to the total number of circuits for which fabrication was begun, may be quite low. Economically, however, the cost of rejecting circuits at an early fabrication step is much lower than rejecting a circuit that fails a final manufacturing test. Therefore, no single yield figure is a complete measure of the economics of a design.

The population from which yield is predicted in this paper is first a population of amplifiers; it is assumed that tantalum circuits to which the amplifiers are appliqued are perfect. Second, the amplifier population already has deleted from it those amplifiers, perhaps entire slices, that have been rejected in fabrication tests meant to insure the integrity of the circuits. Circuits with shorts, opens, etc., have been deleted, and components are within broad tolerance limits, i.e., resistivity measurements insure a ±15 percent spread in resistance values and a variety of tests, including junction breakdown, impose limits on transistor parameters.

In short, the population from which we predict yield is a population of amplifiers each of whose circuits are topologically equivalent to the schematic of Fig. 6 and all of whose parameters are within the limits defined in Ref. 4. It is the population with which one would expect bonding to begin, and, most importantly, the population where failure to meet specification is costly. The yield figure we predict is the yield which is most indicative of the virtue of an electrical design, failures removed prior to construction of our population being process dependent and independent of electrical design.

The outlook for oscillator B is actually brighter than even the 55 percent yield prediction indicates. Four major factors should be considered, viz.,

(*i*) The statistics used to select amplifier parameters were, in general, pessimistic. In this sense, the 55 percent yield figure represents a lower bound. Further, processing improvements which might be expected once the circuit is in full production, especially improvements that increase transistor Betas, will increase yield.

(*ii*) Self-heating of the chip has been ignored in the study. As we shall see, low temperature operation is the limiting condition of the design. Because of self-heating, it is possible that the chip may never operate at −40°C, the lowest expected environmental temperature.

(*iii*) It should be noted that the temperature at which amplitude is adjusted (+20°C) is not centered in the temperature range over

which the oscillator must operate (−40°C to +60°C). Furthermore, amplitude is not a symmetric function of the impairments, e.g., the change in amplitude for negative temperature changes is larger than with positive changes. Hence, a gain in yield may be realized by adjusting amplitude off nominal.

(*iv*) Perhaps most important is that the results of the study show that a simple go/no-go test may be performed on the amplifiers before they are bonded to the tantalum circuits to weed out the 45 percent that fail.

Now to take a detailed look at the results.

### 5.2 *Frequency Stability*

Figure 11 shows the frequency histograms for oscillator B at the temperature extremes. Note that all the oscillators are well within the ±0.1 percent limit. In fact, the oscillators are within ±0.05 percent limits. Hence, as far as frequency is concerned, oscillator B has 100 percent yield. The tight stability has suggested that the notch depth of the Twin-T circuit can be relaxed from 37 dB to 36 dB to ease tantalum fabrication.

### 5.3 *Amplitude Stability*

Figure 12 shows the amplitude histograms at frequency $f_2$,* at the adjustment temperature and at the temperature extremes. Notice that the only failures occur at −40°C. These failures represent 25 percent of the sample amplifiers. Note that all the oscillators meet the adjustment specification by a safe margin.

### 5.4 *Amplitude Change with Tone Frequency*

To examine the change of amplitude with tone change, examine Fig. 13. This figure is a profile of one oscillator; it has 12 data points—four tones, each at three temperatures. Considering the design of the oscillator, one would possibly expect amplitude to increase monotonically with tone frequency. One might argue as follows: The amplifier limits on only one side, and the point of limiting is unaffected by tone change. On the other hand, the base line of oscillation is approximately given by the point on the gain curve where

$$V_2 - R_T I_{dc} = V_1 ,$$

* The oscillator is designed to generate tones of four different frequencies. Henceforth we denote the nominal values of these four frequencies by $f_1$ through $f_4$. $f_1 = 1209$ Hz, $f_2 = 1336$ Hz, $f_3 = 1447$ Hz, and $f_4 = 1633$ Hz. Amplitude is adjusted at $f_2$.

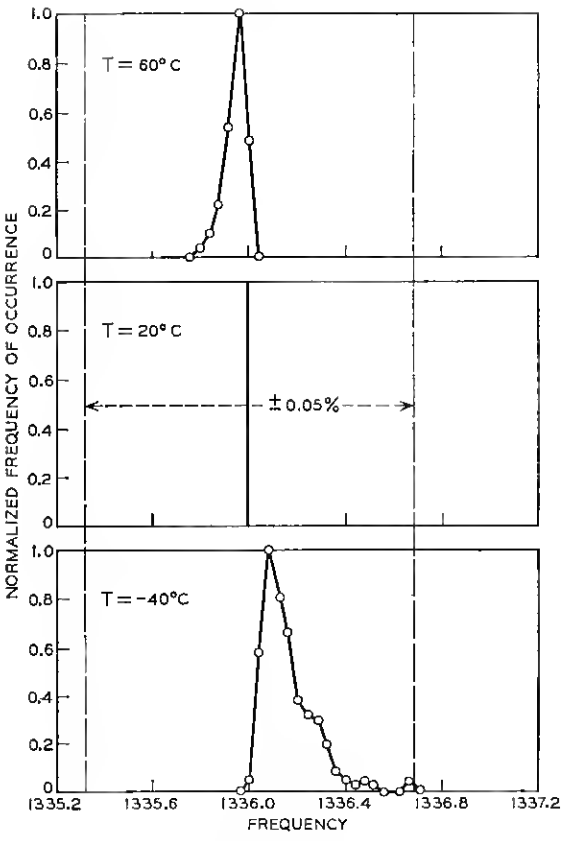


Fig. 11—Amplifier B normalized frequency histograms, $f_0 = 1336$ Hz.

where $R_T$ is the dc resistance of the Twin-T network. $V_2$ and $V_1$ are connected via the amplifier gain, i.e.,

$$V_2 = V_A - KV_1$$

in the linear region, where $V_A$ is some constant and $K$ is the amplifier gain. Then,

$$V_{2\text{dc}} + \frac{V_{2\text{dc}} - V_A}{K} = R_T I_{\text{dc}} ,$$

$$V_{2\text{dc}} \approx V_\alpha + R_T I_{\text{dc}} ,$$

where $V_\alpha$ is the baseline voltage when $I_{\text{dc}} = 0$, the point on the amplifier gain curve where $V_2 = V_1$.

$R_T$ varies inversely with tone frequency, and hence we would expect the center of oscillation to decrease with increasing tone frequency. Since the amplitude is given by the difference between the limiting voltage and the center line voltage, we would expect amplitude to increase monotonically with tone frequency and, assuming constant $I_{dc}$, to be linear at a slope of $-I_{dc}$ with $R_T$. Figure 14 is a plot of amplitude versus $R_T$ with temperature as a parameter. Notice that for $f_1$ to $f_3$ the curves are almost linear but with slopes closer to $-2I_{dc}$. However, when we come to $f_4$, we notice that the curves change direction and violate the monotonicity assumption. One possible explanation for this "turndown" is that the notch of the Twin-T rises monotonically for $f_1$ to $f_3$ and deepens at $f_4$. While this phenomenon

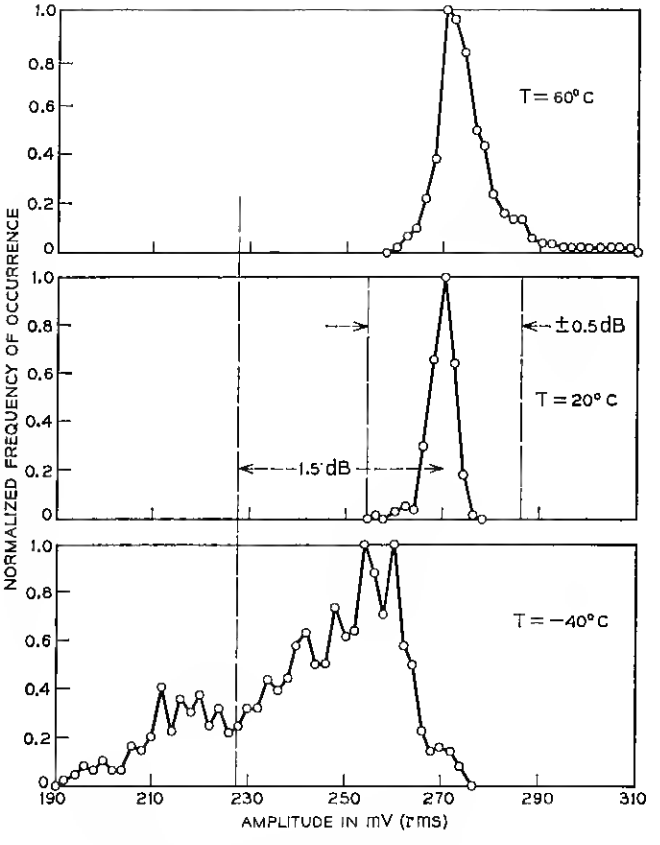


Fig. 12—Amplitude histograms at adjustment frequency.

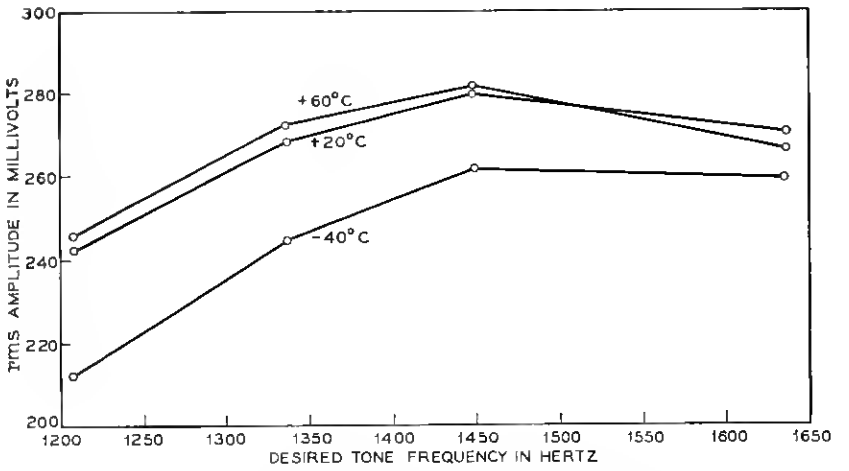


Fig. 13—Amplitude versus frequency profile of one oscillator.

would have a small effect if limiting were perfect, the amplifier under study has exponential limiting. The fact that the notch is deeper at $f_4$ implies that the oscillator does not have to go as far into the exponential limiting region to achieve a loop gain of 0 dB. This effect appears to more than compensate the amplitude growth due to $I_{dc}$. In any case, the amplitude "turndown" has been corroborated by breadboard experiments.

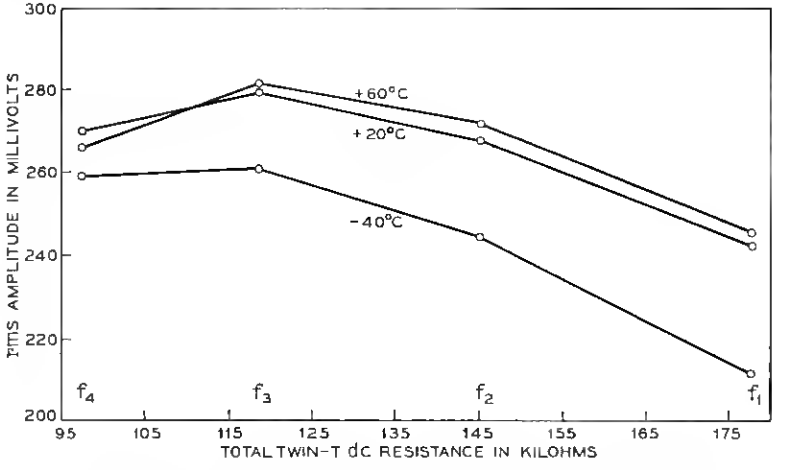


Fig. 14—Amplitude versus Twin-T dc resistance for one oscillator.

Two implications of the non-monotonic relation of amplitude with frequency should be mentioned. First, a linearized, first-order guess, indeed the design assumption, has been proven inaccurate by an analysis which maintains the nonlinear properties of the circuit. Second, since the design specifications place limits on the total amplitude deviation due to tone change, the lack of monotonicity is helpful in meeting specifications.

### 5.5 *Calculation of Yield*

Returning to Fig. 13, we see that the worst-case amplitude deviations due to all causes—adjustment, temperature, tone change—occur at $f_1$, $-40°C$ for negative deviations and $f_3$, $+60°C$ for positive deviations. If we ignore the causes of deviation and simply say that oscillators with amplitudes within $\pm 2.5$ dB (see Section II) of the nominal amplitude for all modes are acceptable, then Fig. 15 allows us to quickly calculate yield. Figure 15 shows the amplitude histograms for $f_1$, $-40°C$ and $f_3$, $+60°C$, with the $-2.5$-dB limit drawn in. The normalized area under the curves outside the 2.5-dB limit represents the fraction of the total amplifiers that fail. Notice that all amplifiers that fail do so at $f_1$, $-40°C$—another indication of the asymmetry of the nominal design. The yield figure is 55 percent.

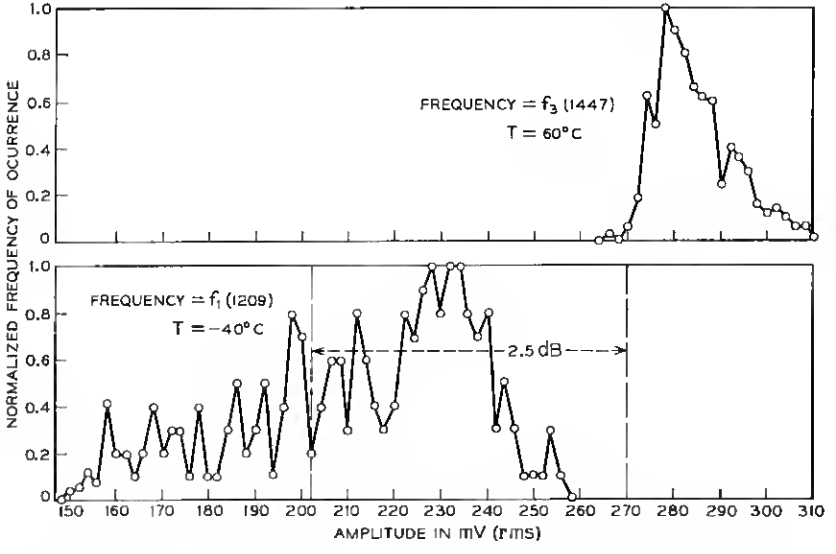


Fig. 15—Amplitude histograms at worst-case conditions. ($f_3$, $+60°C$), ($f_1$, $-40°C$).

### 5.6 *Production Screening Test*

Breadboard experiments and first-order computations had suggested that some level of dc feedback current ($I_{dc}$) could be used as a threshold for production screening of amplifiers. Figure 16 confirms that this is indeed the case and defines the threshold quantitatively. The figure shows maximum amplitude deviation (uniformly this deviation occurs at $f_1$, $-40°C$) versus $I_{dc}$ at $+20°C$ and $f_2$. The close correlation is obvious. If amplifiers with $I_{dc} \geqq 0.4$ $\mu$A are rejected, all remaining amplifiers produce oscillators within design specifications. Note that no temperature tests need be made.

Figure 17 is a histogram of $I_{dc}$. The normalized area under the curve in the interval $[0.4, \infty]$ represents the fraction of amplifiers rejected by the test ($I_{dc} \geqq 0.4$ $\mu$A) and also predicts the same 55 percent yield.

After noting that amplifiers with high $I_{dc}$ have large amplitude deviations, we then ask what causes high $I_{dc}$. Figures 18 and 19 show that low transistor Betas cause high $I_{dc}$ and failures. Figure 18 plots maximum amplitude deviation versus $\beta_{N1} - \beta_N$ of the first transistor. The correlation is barely detectable. The argument here is that $I_{dc}$ is a function of the $\beta_N$s of both transistors one and two as well as other parameters and, although there is correlation between the transistor $\beta_N$s on the same chip, that correlation is not strong enough

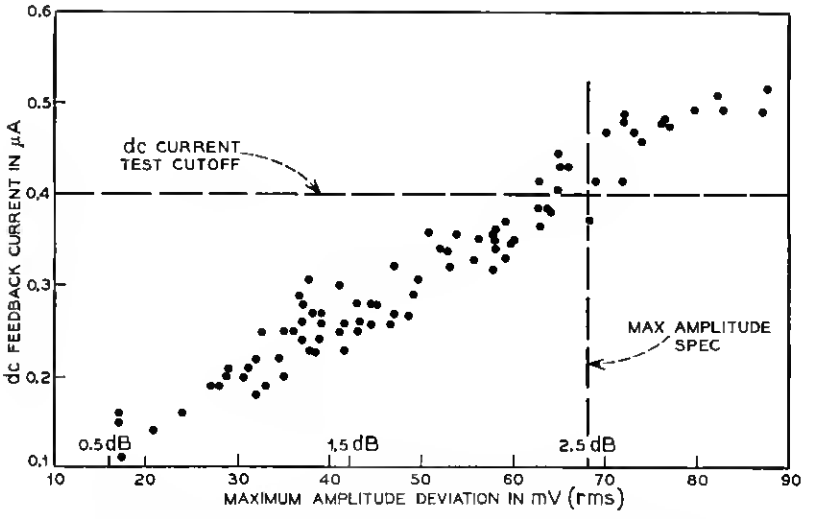


Fig. 16—DC feedback current versus maximum amplitude deviation.

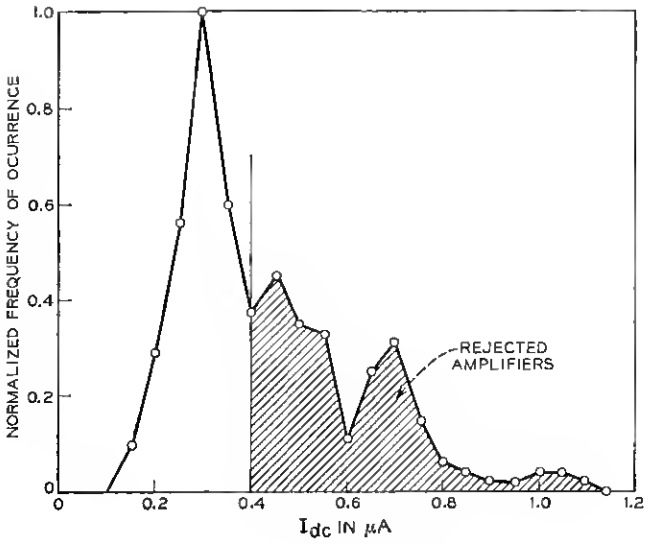


Fig. 17—$I_{dc}$ histogram.

to permit prediction of performance based on measurement of a single transistor $\beta_N$. Figure 19 plots amplitude deviation versus $(\beta_{N1}\beta_{N2})^{\frac{1}{2}}$. Here we see the strong correlation that allows us to draw the conclusion about the dependency of $I_{dc}$ on transistor $\beta_N$ and to predict an improvement in yield if processing improvements result in increased $\beta_N$.

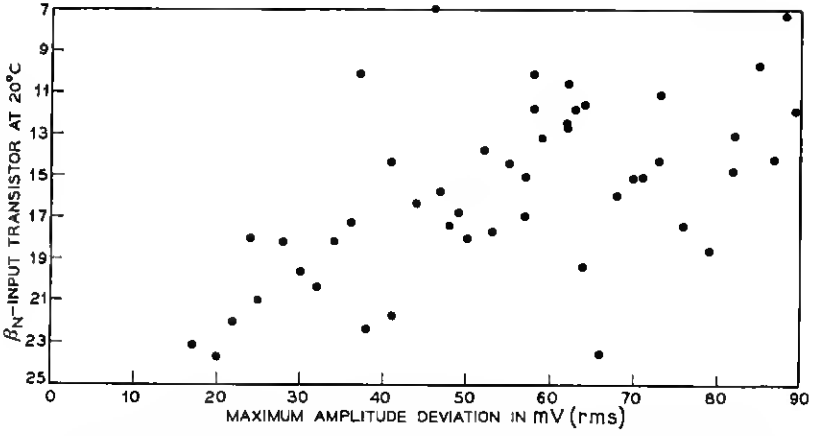


Fig. 18—Maximum amplitude deviation versus $\beta_N$ of input transistor at +20°C.

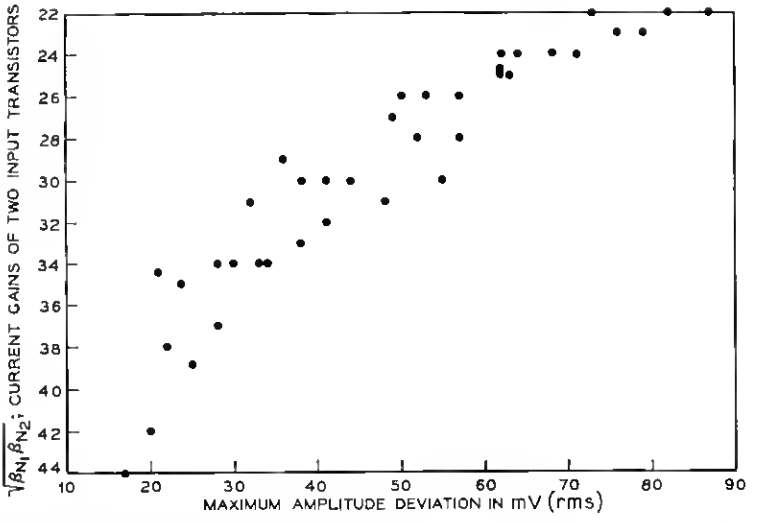


Fig. 19—Maximum amplitude deviation versus $(\beta_{N_1}\beta_{N_2})^{\frac{1}{2}}$. $\beta_{N_1}$, current gain first transistor; $\beta_{N_2}$, current gain second transistor.

Finally, Fig. 20 is a histogram of maximum amplitude deviation with all amplifiers having $I_{dc} \geqq 0.4$ $\mu$A removed. It is clear that all the oscillators in this reduced population are within the design specifications.

### 5.7 *Asymmetric Adjustment*

As a final word, let us return to a discussion of the asymmetry of the nominal design. For amplitude adjustment at 20°C and $f_2$, a first guess for the adjustment target was nominal amplitude. An adjustment temperature of 20°C is higher than the center of the operational temperature range (−40°C to +60°C), and for this reason one might consider adjusting amplitude at a higher value than nominal. However, $f_2$ is lower than the center of the frequency range, and if one accepted the notion of amplitude varying proportionally with frequency, one might consider adjusting to an amplitude below nominal. These two factors then tend to cancel one another.

The results presented previously, however, indicate that amplitude is not a monotonic function of frequency, and amplitude deviations due to both temperature and frequency changes are asymmetric. We have shown that larger variations in amplitude result from negative changes in temperature and frequency than from positive changes.

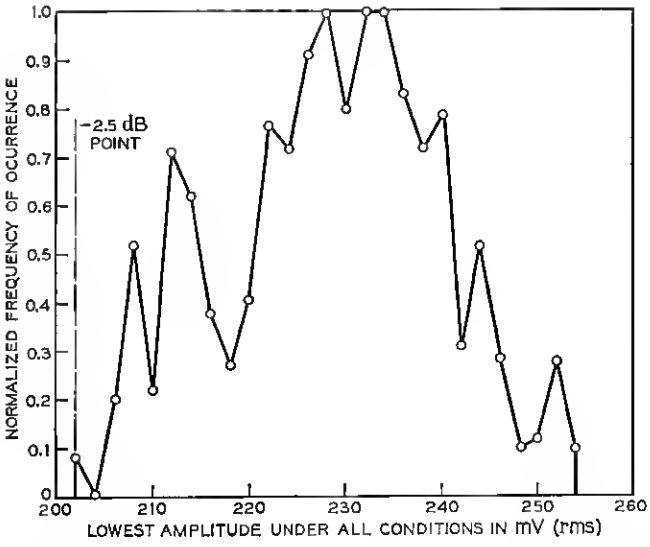


Fig. 20—Histogram of lowest amplitude from all conditions, amplifiers with $I_{dc} \geqq 0.4$ μA removed.

We have seen that the dominant failure condition is $f_1$, −40°C, i.e., low tone frequeney, low temperature. This suggests that amplitude can be adjusted to take advantage of the asymmetry. If adjusting at $f_2$ and +20°C, an adjustment objective of 285 mV rather than 270 mV is likely to result in increased yield, i.e., it will be possible to accept amplifiers with $I_{dc}$ greater than 0.4 μA. Although the exact adjustment figure must still be studied, our results suggest that taking advantage of the asymmetry of the design can result in not insignificant savings.

## VI. CONCLUSIONS

In this paper we have deseribed the application of Monte Carlo tolerance analysis to the integrated, single-substrate, RC, *Touch-Tone* oscillator. The conclusions to be drawn are pertinent not only to the specific oscillator designs studied, but also to the state-of-the-art of toleranee analysis itself.

We have examined two proposed oscillator designs. Both designs employ the same Twin-T as the frequency selective network, the difference appearing in the high-gain, limiting amplifier. The study, therefore, eoneentrated on the statistieal variation of parameter values within the amplifier; the Twin-T was held fixed at design values.

Variations in oscillator performance, then, were judged against degradation limits allocated to the amplifier.

The first design was dismissed because of poor frequency stability stemming from loading effects of the amplifier on the Twin-T. The second design, on the other hand, seems promising; its production now seems likely.* The Monte Carlo analysis of this design revealed two significant properties:

First, the oscillator has excellent frequency stability. Frequency deviations over the full temperature range were less than 0.05 percent for all the sample oscillators in the Monte Carlo study.

Second, the amplitude stability is acceptable. Fifty-five percent of the oscillators in the study were within amplitude limits over the full temperature and tone frequency ranges. Forty-five percent of the oscillators failing specifications is less alarming than might appear at first glance for the following reasons:

(*i*) The results show that amplitude deviations are strongly correlated with the dc feedback current through the Twin-T, i.e., into the amplifier, at room temperature. Hence a test is easily performed on the amplifier chips before bonding takes place and without the need of a temperature chamber to weed out amplifiers that would result in unsatisfactory oscillators. This test reduces the cost penalties associated with a relatively low amplifier yield.

(*ii*) The statistical characterization of the parameters of the oscillator was purposely pessimistic. Hence, the yield figure should be taken as a lower bound. Further, the results indicate that amplifier failure is associated with low transistor current gain. Fabrication improvements that increase these gains will therefore improve yield.

(*iii*) The deviation of oscillator amplitude in response to both temperature and tone change is asymmetric, i.e., amplitude deviations due to both low temperature and lower frequency is larger than corresponding changes for high temperature and higher frequency. By changing the amplitude adjustment target to some value offset from the middle of the amplitude window (270 mV $\pm$ 2.5 dB), a significant increase in yield can be expected.

In summary, amplifier yield of 55 percent is lower than might be

* It should be noted that several potential problem areas have been ignored in the computer analysis and remain to be examined. Primary among these are the effects of variable loop length and the possibility of parasitic oscillation.

hoped for, but the cost penalties associated with this relatively low yield are minimized by a simple go/no-go test performed on the amplifiers before bonding. Furthermore, there are good prospects that yield can be increased by changes in silicon processing and adjustment strategy.

With regard to Monte Carlo tolerance analysis itself, two aspects of the present study should be noted. First, since the oseillator is nonlinear and requires factory adjustment, no standard circuit analysis program could reasonably be used as part of a Monte Carlo loop. Hence, a special program in which efficiency could be achieved by restricting its applicability to a small class of oscillators had to be written. To write this program required one man-year of effort—a not unsubstantial investment. The point is that while Monte Carlo tolerance analysis of eireuits like the *Touch-Tone* oscillator cannot, at present, be performed using off-the-shelf computer programs, the analysis can be done using special techniques if the circuit's importance warrants the investment.

Secondly, since the oscillator's amplifier is fabricated on a single silieon ehip, its parameters are not statistically independent. Unfortunately, almost no data exists with which to make a statistical characterization of silicon circuit parameters. On the other hand, it is obvious that the results of the Monte Carlo study are exactly as accurate as the assumed parameter statistics. It is clear, then, that if we are to exploit the possibilities Monte Carlo tolerance analysis presents, an effort must be made to structure the measurements of silicon circuits as they go into production, to clarify the statistical interrelation of silicon circuit parameters.

## VII. ACKNOWLEDGMENT

The help of many people in providing device characterization, circuit expertise, and their insight into the problems of producing a single-substrate, *Touch-Tone* dial is gratefully asknowledged. Without being exhaustive, L. A. Walter supplied most of the device data from which J. Logan produced the statistical characterization and technique for parameter selection;[4] T. L. Powers, D. P. Borenstein, J. H. Hamm and R. A. Tice shared their experience with previous *Touch-Tone* dials and their insight into the problems of the new circuits, and coordinated their own laboratory work with the computer analysis; W. H. Orr and P. Zuk provided details of the fabrication process and their own views of the circuit operation; R. W. Wyndrum, Jr., and

T. N. Rao introduced us to the problem; and J. Chernak provided leadership that kept us excitedly at our task.

REFERENCES

1. Dickieson, A. C., and Chernak, J., "History and Introduction," B.S.T.J., this issue, pp. 1099–1103.
2. Semmelman, C. L., Walsh, E. D., and Daryanani, G. T., "Linear Circuits and Statistical Design," B.S.T.J., this issue, pp. 1149–1171.
3. Cermak, I. A., and Kirby, Mrs. D. B., "Nonlinear Circuits and Statistical Design," B.S.T.J., this issue, pp. 1173–1195.
4. Logan, J., "Characterization and Modeling for Statistical Design," B.S.T.J., this issue, pp. 1105–1147.
5. Shichman, H., "Integration System of a Nonlinear Network Analysis Program," IEEE Trans. Circuit Theory, *CT-17*, No. 3 (August 1970), pp. 378–385.